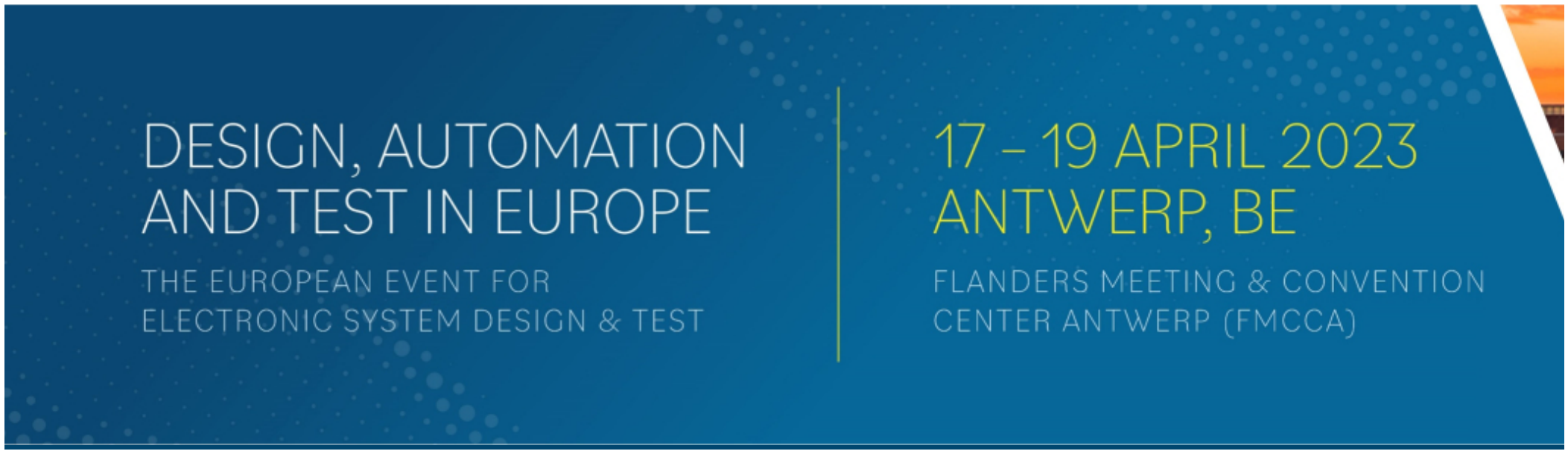

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Wed, 19 Apr 2023 18:49

DATE 2023 Awards

2023 EDAA Achievement Award

Jason Cong, UCLA, US

https://www.date-conference.com/edaa-achievement-award-2023-goes-jason-cong

IEEE CEDA Service Award

Cristiana Bolchini, Politecnico di Milano, IT

ESDA / CEDA Phil Kaufman Award 2022:

Giovanni De Micheli, EPFL, CH

IEEE CS TTTC Outstanding Contribution Award

Ian O'Connor, École Centrale de Lyon, FR

ACM SIGDA/CEDA/EDAA PhD Forum Prize

Alessio Burrello, Politecnico di Torino and Università di Bologna, IT

Optimizing Ai: From Network Topology Design To Mcu Deployment

Jatin Arora, CISTER Research Centre, ISEP, IPP, PT

Shared Resource Contention Aware Schedulability Analysis For Multiprocessor Real-Time Systems

EDAA Outstanding Dissertations Award 2023

Topic 1:

Xiaochen Peng, Ph.D

Benchmark Framework for 2-D/3-D Integrated Compute-in-Memory based Machine Learning Accelerator

Topic 2:

Martin Rapp, Ph.D.

Machine Learning for Resource-Constrained Computing Systems

Topic 3:

Zhiyao Xie, Ph.D.

Intelligent Circuit Design and Implementation with Machine Learning

Topic 4:

Hasan Hassan, Ph.D.

Improving DRAM Performance, Reliability, and Security by Rigorously Understanding Intrinsic DRAM operations

DATE Fellow Award 2023

Cristiana Bolchini, Politecnico di Milano, IT

DATE 2023 also presented the DATE Fellow Awards from DATE 2020 to DATE 2022:

DATE Fellow Award 2020: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

DATE Fellow Award 2021: Giorgio di Natale, LIRMM, Montpellier, FR

DATE Fellow Award 2022: Franco Fummi, University of Verona, IT

DATE Best Paper Awards 2023

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee composed of the Track Chairs Lukas Sekanina, Alberto Bosio, Ilia Polian and Liliana Cucu and the following members: Katell Morin-Allory, Jeronimo Castrillon, Alessio Spessot, Julio Medina, Jean-Philippe Noel, Lorena Anghel, Dimitris Gizopoulos, Rosa Rodríguez-Montañés, Kazuo Sakiyama, Elke De Mulder, Ahmed Rezine, Cristiana Bolchini, Callie Cong, Julien Forget and Masanori Hashimoto.

D-Track

Hardware Efficient Weight-Binarized Spiking Neural Networks

Chengcheng Tang and Jie Han

University of Alberta, CA

A-Track

Automated Energy-Efficient DNN Compression under Fine-Grained Accuracy Constraints

Ourania Spantidi and Iraklis Anagnostopoulos

Southern Illinois University Carbondale, US

T-Track

SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility

Haoyi Zhang, Xiaohan Gao, Haoyang Luo, Jiahao Song, Xiyuan Tang, Junhua Liu, Yibo Lin, Runsheng Wang and Ru Huang

Peking University, CN

E-Track

PRADA: Point Cloud Recognition Acceleration via Dynamic Approximation

Zhuoran Song, Heng Lu, Gang Li, Li Jiang, Naifeng Jing and Xiaoyao Liang

Shanghai Jiao Tong University, CN

Best Paper Award Nominations

D Track

Perspector: Benchmarking Benchmark Suites

Sandeep Kumar1; Abhisek Panda2; Smruti R. Sarangi1

1IIT Delhi, IN; 2Indian Institute of Technology, IN

A Speed- and Energy-Driven Holistic Training Framework for Sparse CNN Accelerators

Yuanchen Qu; Yu Ma; Pingqiang Zhou

Shanghaitech University

GraphIte: Accelerating Iterative Graph Algorithms on ReRAM Architectures via Approximate Computing

Dwaipayan Choudhury; Ananth Kalyanaraman; Partha Pratim Pande

Washington State University

Narrowing The Synthesis Gap: Academic FPGA Synthesis Is Catching Up With The Industry

Benjamin Barze1; Arya Reais-Parsi1; Eddie Hung2; Minwoo Kang1; Alan Mishchenko1; Jonathan W. Greene1; John Wawrzynek1

1UC Berkeley, US; 2FPG-eh Research and University of British Columbia

Computing Effective Resistances on Large Graphs Based on Approximate Inverse of Cholesky Factor

Zhiqiang Liu; Wenjian Yu

Tsinghua University

Fanout-Bounded Logic Synthesis for Emerging Technologies - A Top-Down Approach

Dewmini Marakkalage; Giovanni De Micheli

Ecole Polytechnique Fdrale de Lausanne (EPFL)

Hardware Efficient Weight-Binarized Spiking Neural Networks

Chengcheng; Jie Han

University of Alberta

Hierarchical Non-Structured Pruning for Computing-In-Memory Accelerators with Reduced ADC Resolution Requirement

Wenlu Xue; Jinyu Bai; Sifan Sun; Wang Kang

Beihang University

PIC-RAM: Process-Invariant Capacitive Multiplier Based Analog In Memory Computing in 6T SRAM

Kailash Prasad; Aditya Biswas; Arpita Kabra; Joycee Mekie

Indian Institute of Technology Gandhinagar

Benchmarking Large Language Models for Automated Verilog RTL Code Generation

Shailja Thakur1; Baleegh Ahmad1; Zhenxing Fan1; Hammond Pearce1; Benjamin Tan2; Ramesh Karri1; Brendan Dolan-Gavitt1; Siddharth Garg1

1New York University; 2University of Calgary

Processor Verification using Symbolic Execution: A RISC-V Case Study

Niklas Bruns1; Vladimir Herdt2; Rolf Drechsler1,2

1University of Bremen, 2DFKI

Synthesis with Explicit Dependencies

Priyanka Golia1,2; Subhajit Roy1; Kuldeep S Meel2

1IIT Kanpur, 2National University of Singapore

Minimizing Communication Conflicts in Network-On-Chip based Processing-In-Memory Architecture

Hanbo Sun; Tongxin Xie; Zhenhua Zhu; Guohao Dai; Huazhong Yang; Yu Wang

Tsinghua University

Accelerating Gustavson-based SpMM on Embedded FPGAs with Element-wise Parallelism and Access Pattern-aware Caches

Shiqing Li; Weichen Liu

Nanyang Technological University

PEDAL: A Power Efficient GCN Accelerator with Multiple DAtafLows

Yuhan Chen; Alireza Khadem; Xin He; Nishil Talati; Tanvir Ahmed Khan; Trevor Mudge

University of Michigan

SAGERoute: Synergistic Analog Routing Considering Geometric and Electrical Constraints with Manual Design Compatibility

Haoyi Zhang; Xiaohan Gao; Haoyang Luo; Jiahao Song; Xiyuan Tang; Junhua Liu; Yibo Lin; Runsheng Wang; Ru Huang

Peking University

Non-Profiled Side-Channel Assisted Fault Attack: A Case Study on DOMREP

Sayandeep Saha; Prasanna Ravi; Dirmanto Jap; Shivam Bhasin

Nanyang Technological University, Singapore

Efficient Software Masking of AES through Instruction Set Extensions

Songqiao Cui; Josep Balasch

KU Leuven

Hardware Trojans in eNVM Neuromorphic Devices

Lingxi Wu; Rahul Sreekumar; Rasool Sharifi; Kevin Skadron; Stan Mircea; Ashish Venkat

University of Virginia

SoCFuzzer: SoC Vulnerability Detection using Cost Function enabled Fuzz Testing

Muhammad Monir Hossain; Arash Vafaei; Kimia Zamiri Azar; Fahim Rahman; Farimah Farahmandi; Mark Tehranipoor

University of Florida

A Track

Automated Energy-Efficient DNN Compression under Fine-Grain Accuracy Constraints

Ourania Spantidi; Iraklis Anagnostopoulos

Southern Illinois University Carbondale

Efficient Parallelization of 5G-PUSCH on a Scalable RISC-V Manycore Processor

Marco Bertuletti1; Yichao Zhang1; Alessandro Vanelli-Coralli1,2; Luca Benini1,2

1ETH Zurich; 2Universita di Bologna

EvoLUTe: Evaluation of Look-Up-Table-based Fine-Grained IP Redaction

Rui Guo; Mohammad Rahman; Hadi Mardani Kamali; Fahim Rahman; Farimah Farahmandi;

Mark Tehranipoor University of Florida

RTLock: IP Protection using Scan-Aware Logic Locking at RTL

Md Rafid Muttaki; Shuvagata Saha; Hadi Mardani Kamali; Fahim Rahman; Mark Tehranipoor;

Farimah Farahmandi

University of Florida

CorrectNet: Robustness Enhancement of Analog In-Memory Computing for Neural Networks by Error Suppression and Compensation

Amro Eldebiky1; Grace Li Zhang2; Georg Bocherer3; Bing Li1; Ulf Schlichtmann1

1Technical University of Munich; 2TU Darmstadt; 3Huawei Munich Research Center

T Track

Device-Aware Test for Back-Hopping Defects in STT-MRAMs

Sicong Yuan1; Mottaqiallah Taouil1; Moritz Fieback1; Hanzhi Xun1; Erik Jan Marinissen2; Gouri Kar2; Siddharth Rao2; Sebastien Couet2; Said Hamdioui1

1Delft University of Technology; 2IMEC

Assessing Convolutional Neural Networks Reliability through Statistical Fault Injections

Annachiara Ruospo1; Gabrile Gavarini1; Corrado De Sio1; Juan Guerrero Balaguera1; Luca Sterpone1; Matteo Sonza Reorda1; Ernesto Sanchez1; Riccardo Mariani2; Joseph Aribido2;

Jyotika Athavale2 1Politecnico di Torino; 2NVIDIA

E Track

Light Flash Write for Efficient Firmware Update on Energyharvesting IoT Devices

Songran Liu1; Mingsong Lv2; Wei Zhang3; Xu Jiang1; Chuancai Gu4; Tao Yang4; Wang Yi5; Nan Guan6

1Northeastern University; 2The Hong Kong Polytechnic University; 3Shandong University; 4Huawei Technologies Company; 5Uppsala University; 6City University of Hong Kong

Ditty: Directory-based Cache Coherence for Multicore Safety-critical Systems

Zhuanhao Wu; Marat Bekmyrza; Nachiket Kapre; Hiren Patel

University of Waterloo

PRADA: Point Cloud Recognition Acceleration via Dynamic Approximation

Zhuoran Song; Heng Lu; Gang Li; Li Jiang; Naifeng Jing; Xiaoyao Liang

Shanghai Jiao Tong University

Federated Learning with Heterogeneous Models for On-device Malware Detection in IoT Networks

Sanket Shukla1; Setareh Rafatirad2; Houman Homayoun2; Sai Manoj Pudukotai Dinakarrao1 1George Mason University; 2University of California Davis

Genetic Algorithm-based Framework for Layer-Fused Scheduling of Multiple DNNs on Multi-core Systems

Sebastian Karl1; Arne Symons2; Nael Fasfous; Marian Verhelst2

1TU Munich; 2KU Leuven; 3BMW AG

HADAS: Hardware-Aware Dynamic Neural Architecture Search for Edge Performance Scaling

Halima Bouzidi1; Mohanad Odema2; Hamza Ouarnoughi3; Mohammad Al Faruque2; Smail Niar3

1Univ. Polytechnique Hauts-de-France, LAMIH; 2University of California Irvine; 3INSA Hautsde-France

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Tue, 18 Apr 2023 15:00

Survey: Conference Evaluation, Suggestions & Comments

This survey is available from Monday, 17 April 2023, 15:00 CEST to Friday, 21 April 2023, 17:00 CEST.

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date-registration@kitdresden.de

Tue, 28 Feb 2023 11:38

EDAA Achievement Award 2023 goes to Jason Cong

The Achievement Award is given to individuals who made outstanding contributions to state of the art in electronic design, automation and testing of electronic systems in their life. To be eligible, candidates must have made innovative contributions that impacted how electronic systems are being designed.

Past recipients have been Kurt ANTREICH (2003), Hugo DE MAN (2004), Jochen JESS (2005), Robert BRAYTON (2006), Tom W. WILLIAMS (2007), Ernest S. KUH (2008), Jan M. RABAEY (2009), Daniel D. GAJSKI (2010), Melvin A. BREUER (2011), Alberto L. SANGIOVANNI-VINCENTELLI (2012), Peter MARWEDEL (2013), Rolf ERNST (2014), Lothar THIELE (2015), Giovanni DE MICHELI (2016), C. L. David LIU (2017), Mary Jane IRWIN (2018), Jacob ABRAHAM (2019), Luca BENINI (2020), Georges GIELEN (2021), and Edward A. LEE (2022).

Dr. Jason Cong is the Volgenau Chair for Engineering Excellence in the UCLA Computer Science Department (with a joint appointment in the Department of Electrical and Computer Engineering), the Director of the Center for Domain-Specific Computing (funded by NSF Expeditions in Computing Award), and the director of VLSI Architecture, Synthesis, and Technology (VAST) Laboratory. He served as the chair of the UCLA Computer Science Department from 2005 to 2008. He is the author of more than 500 papers, including 17 Best Paper Awards. Dr. Cong's research publications have close to 35,000 citations, according to Google Scholar, and he is a frequent keynote speaker at major conferences in EDA and design automation. He has graduated 44 PhD students.

Download further information:
EDAA Press Release - EDAA Achievement Award 2023 goes to Jason Cong (288.23 KB)

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Fri, 10 Feb 2023 14:23

DATE Programme Overview

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Week Day

Friday, 21 April 2023

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09:30

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- In cooperation with Visit Antwerp, Antwerp city pass are offered at discounted prices for DATE 2023 delegates.

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We would be delighted to welcome you among our promotion partners and sponsors at DATE, and to welcome you in Antwerp for an interesting programme and effective networking.

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Thu, 20 Oct 2022 16:59

Careers Fair - Industry - Call for Submissions

Information for Students

The Young People Programme aims at bringing together Ph.D./Master Students and potential job seekers with recruiters from EDA and microelectronic companies. Interested jobseekers have the opportunity to apply to open positions which will be presented by the companies. If a student raises the interest in the position, an interview will be scheduled.

Eligibility

The following two classes of students are eligible:

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OK_1 Opening Keynote 1: Building the Metaverse: Augmented Reality applications and integrated circuit challenges

Start: Mon, 09:00

Edith Beigné, Meta Reality Labs, United States

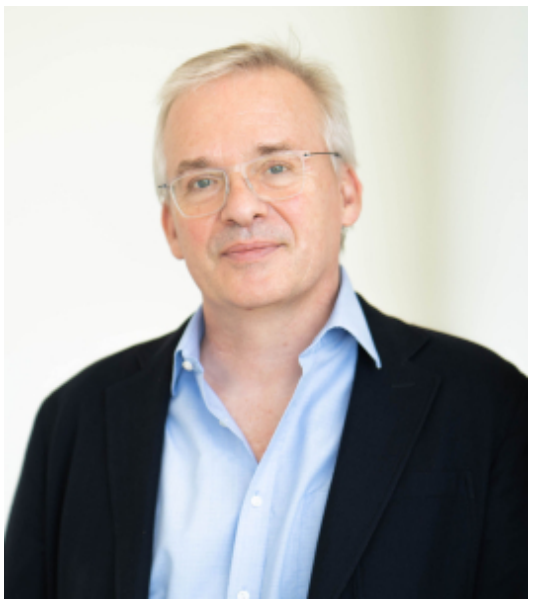
Abstract: Augmented reality is a set of technologies that will fundamentally change the way we interact with our environment. It represents a merging of the physical and the digital worlds into a rich, context aware and accessible user interface delivered through a socially acceptable form factor such as eyeglasses. One of the biggest challenges in realizing a comprehensive AR experience are the performance and form factor requiring new custom silicon. Innovations are mandatory to manage power consumption constraints and ensure both adequate battery life and a physically comfortable thermal envelope. This presentation reviews Augmented Reality and Virtual Reality applications and Silicon challenges.

Read more

OK_2 Opening Keynote 2: The Cyber-Physical Metaverse – Where Digital Twins and Humans Come Together

Start: Mon, 09:45

Dirk Elias, Robert Bosch GmbH, Germany



Abstract: The concept of Digital Twins (DTs) has been discussed intensively for the past couple of years. Today we have instances of digital twins that range from static descriptions of manufacturing data and material properties to live interfaces to operational data of cyber physical systems and the functions and services they provide.

Currently, there are no standardized interfaces to aggregate atomic DTs (e.g., the twin of the lowest-level function of a machine) to higher-level DTs providing more complex services in the virtual world. Additionally, there is no existing infrastructure to reliably link the DTs in the virtual world to the integrated CPSs in the real world (like a car consisting of many ECUs with even more functions).

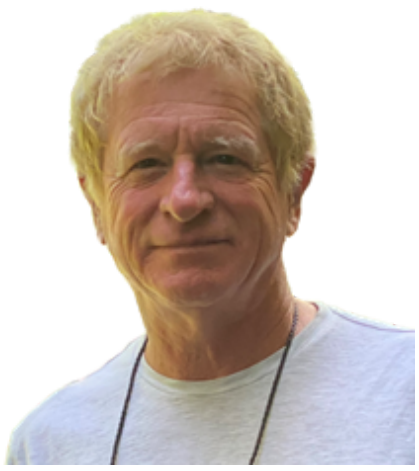
This keynote will address how the Metaverse can become the virtual world where DTs of humans and machines live and how to reliably connect DTs to the physical world. Insights in current activities of Bosch Research and its academic partners to move towards this vision will be provided.

Read more

LK_1 IEEE CEDA Distinguished Lecturer Lunchtime Keynote: Restoring the magic in design

Start: Mon, 13:00

Jan M. Rabaey, University of California at Berkeley, United States and imec, Belgium



Abstract: The emergence of “Very Large Scale Integration (VLSI)” in the late 1970’s created a groundswell of feverish innovation. Inspired by the vision laid out in Mead and Conway’s “Introduction to VLSI Design”, numerous researchers embarked on venues to unleash the capabilities offered by integrated circuit technology. The introduction of design rules, separating manufacturing from design, combined with an intermediate abstraction language (CIF) and a silicon brokerage service (MOSIS) gave access to silicon for a large population of eager designers. The magic however expanded way beyond these circuit enthusiasts and attracted a whole generation of software experts to help automate the design process, given rise to concepts such as layout generation, logic synthesis, and silicon compilation. It is hard to overestimate the impact that this revolution has had on information technology and society at large.

About fifty years later, Integrated Circuits are everywhere. Yet, the process of creating these amazing devices feels somewhat tired. CMOS scaling, the engine behind the evolution in complexity over all these decades, is slowing down and will most likely peter out in about a decade. So has innovation in design tools and methodologies. As a consequence, the lure of IC design and design tool development has faded, causing a talent shortage worldwide. Yet, at the same time, this moment of transition offers a world of opportunity and excitement. Novel technologies and devices, integrated in three-dimensional artifacts are emerging and are opening the door for truly transformational applications such as brain-machine interfaces and swarms of nanobots. Machine learning, artificial intelligence, optical and quantum computing present novel models of computation surpassing the instruction-set processor paradigm. With this comes a need again to re-invent the design process, explicitly exploiting the capabilities offered by this next generation of computing systems. In summary, it is time to put the magic in design again.

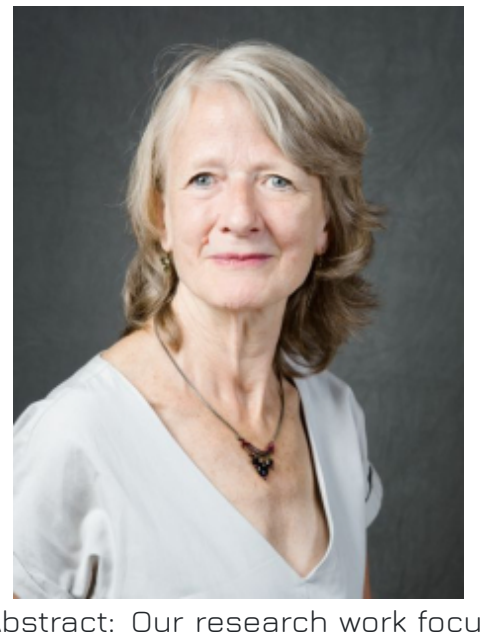
Read more

LK_2 Special Day Lunchtime Keynote: Interacting with Socially Interactive Agent

Start: Tue, 13:00

Catherine Pelachaud, CNRS-ISIR, Sorbonne Université,

France



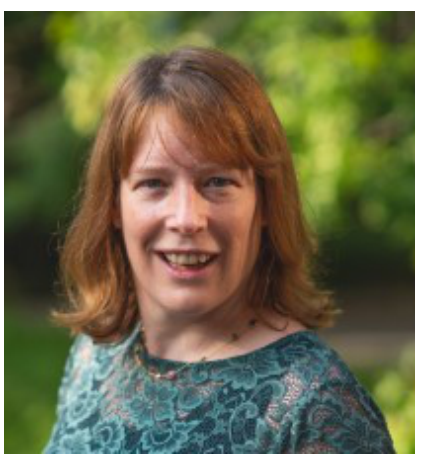
Abstract: Our research work focuses on modeling Socially Interactive Agents, i.e. agents capable of interacting socially with human partners, of communicating verbally and non-verbally, of showing emotions. but also of adapting their behaviors to favor the engagement of their partners during the interaction. As partner of an interaction, SIA should be able to adapt its multimodal behaviors and conversational strategies to optimize the engagement of its human interlocutors. We have developed models to equip these agents with these communicative and social abilities. In this talk, I will present the works we have been conducted.

Read more

LK_3 Special Day Lunchtime Keynote: Analyze the Patient, engineer the therapy

Start: Wed, 13:00

Liesbet Lagae, KU Leuven, Belgium



Abstract: The complexity, cycle time and cost of new precision therapy workflow are a major challenge to overcome in order to achieve clinical implementation of this revolutionary type of treatments. For example, car T cells use the patient's own immune (T-)cell adapted in a way to better fight cancer. Chip technology can help to make these therapies more efficient, precise, and cost-effective. Over the last few decades, the semiconductor industry has grown exponentially, poised to increase value to the end-user while driving down costs by scaling. The result is the world's highest standard in precision and high-volume production of nanoelectronics chip-based sensor solutions. Imec has used its semiconductor process expertise and infrastructure to make significant innovations in single-use silicon biochip and microfluidic technology, creating toolboxes of on-chip functions spanning DNA sequencing, cell sorting, single cell electroporation, integrated biosensor arrays. The solutions have until now mostly served the diagnostic market. Chip based microfluidics is a toolbox that brings its own design challenges, especially in relation to not having to reinvent the wheel every time. Hence, we try to make maximal reuse of generic fluidic building blocks developed for the diagnostic market, and we will explain how these building blocks are equally adapted for addressing the challenges in immune therapy. These existing demonstrations on chip could enable to provide smarter solutions for discrete unit operations and quality monitoring to even complete workflow integration. Solving these challenges would enable more patients to access and benefit from the next most anticipated class of life changing therapies.

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