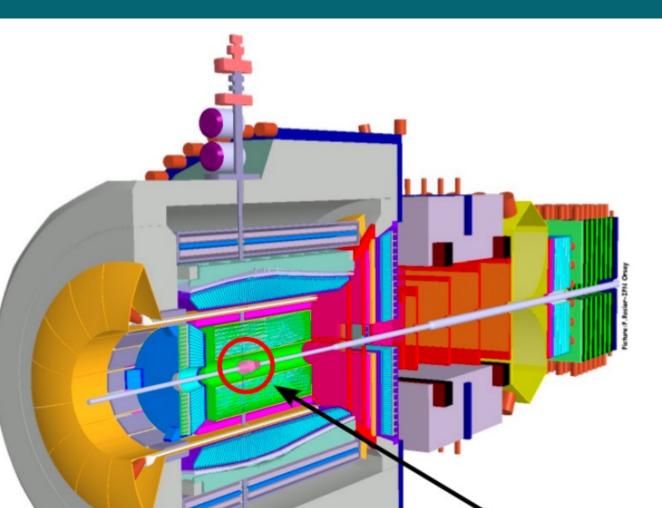


38th Cycle

ToAST: a 64 channels ASIC for the readout of the silicon strip detectors Francesca Lenta Supervisor: Mazza G., Rivetti A., Goano M.

Research context and motivation

- **PANDA experiment** located at the **FAIR** facility in Darmstadt
- Antiproton-proton and antiproton-nuclei annihilation reactions
- Fixed target (a target pipe intersects the beam pipe)
- **Barrel region** : 2 layers of Silicon Pixel Detectors (SPDs) + 2 of Silicon Strip Detectors (SSDs)
- Forward region : 4 SPDs disks, 2 SPDs + SSDs disks
- Triggerless experiment

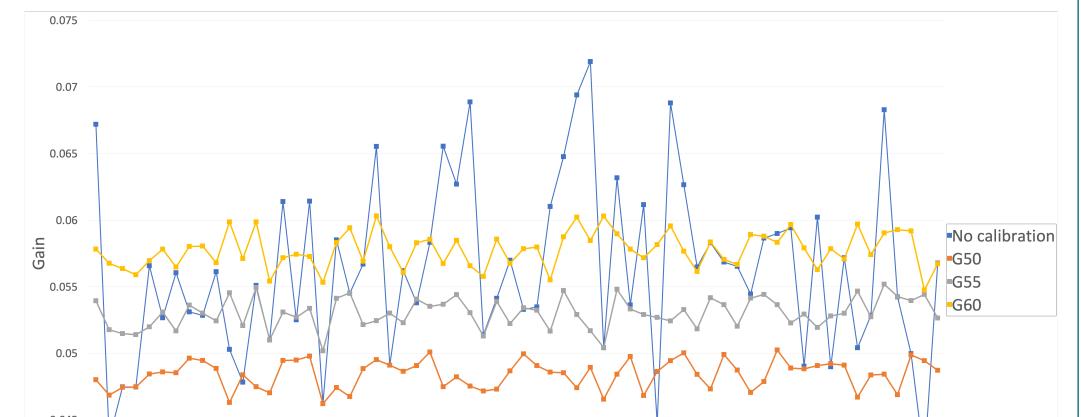


MVD

Novel contributions

Characterization of the ToASt ASIC v1

Gain and ToT offset calibration • ToT programmable Gain between 50 to 60 ns/fC for both polarities

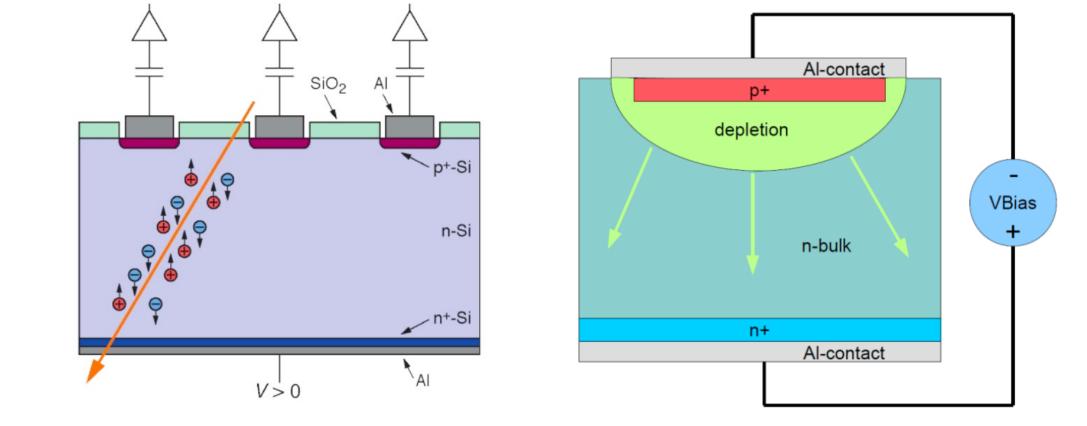


Addressed research questions/problems

Necessary to design a new ASIC due to triggerless experiment \rightarrow there is not an external signal that validates the data in a certain time interval and all must be transmitted

Double side SSDs :

- Doped silicon semiconductor
- PN-junction
- Reverse bias voltage
- Breakdown voltage > 200 V
- Depletion voltage \approx 100 V

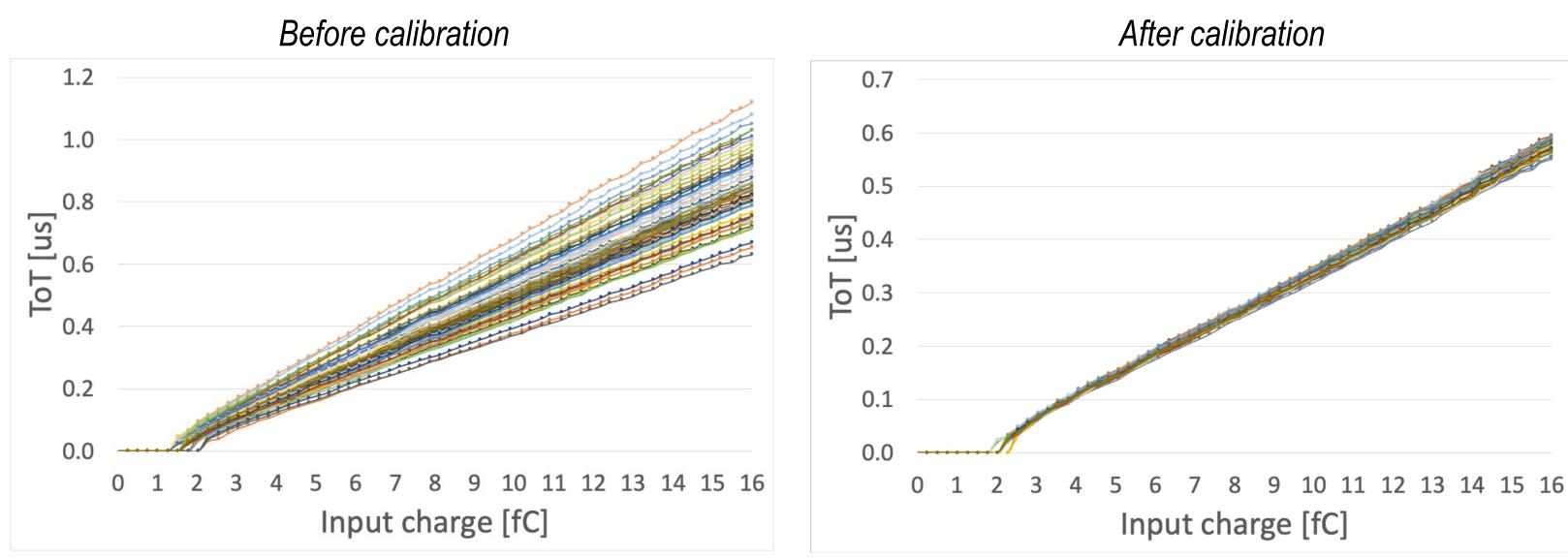


SSDs readout requirements:

Channels per chip	64
• •	
Charge resolution	8 bits
Input charge	1 – 40 fC
Noise	max 1500 e ⁻
Reference clock	160 MHz
Power consumption	max 256 mW
Radiation tollerance	20 kGy
Chip dimentions	4.5 x 3.5 mm ²

Calibration procedure:

- For each channel, measure the transfer curve for each channel ToT Ibias DAC value
- Select a reference gain
- For each channel, select the DAC value providing the gain closest to the reference
- For each channel, measure the offset of the ToT
- Select a reference offset
- For each channel, select the DAC value providing the offset closest to the reference



Noise

Scan performed with a fixed number of pulses and changing the threshold

 $f(x') = \frac{N}{2} \left(1 + \frac{2}{\sigma\sqrt{\pi}} \int_0^{x'} exp(-s^2) dx \right) , \ s = \frac{x-\mu}{\sigma}$

Adopted methodologies

nannels 63-56

ToASt specifics and architecture:

- Commercial 110 nm CMOS technology
- Triplicated logic to protect against single event upsets
- 64 readout channels
- 8 regions with local FIFO
- Each channel provides the ToA and the charge measurement
- 160MHz clock
- Two 160 Mb/s serial lines
- Configuration serial link running at half the master clock frequency (80 Mb/s)
- Fully digital interface in order to avoid the transmission of noise sensitive analog signals

olitecnico

di Torino

Configuration Unit Channels 55-48 Region 6 80 Mb/s Channels 47-40 Region 5 configuration registers Channels 39-32 Region 4 Address Channels 31-24 Region 3 PonRstb RstSync Channels 23-16 Region 2 **≺**—*Clock* Channels 15-7 Region 1 TestP Global R/O Unit Channel 7 Region 0 Channel 6 Readout Unit Channel 5 160 Mb/s Channel 4 64 cells FIFO Channel 3 160 Mb/s Channel 2 Configuration Channel 1 Unit Channel 0

Region 7

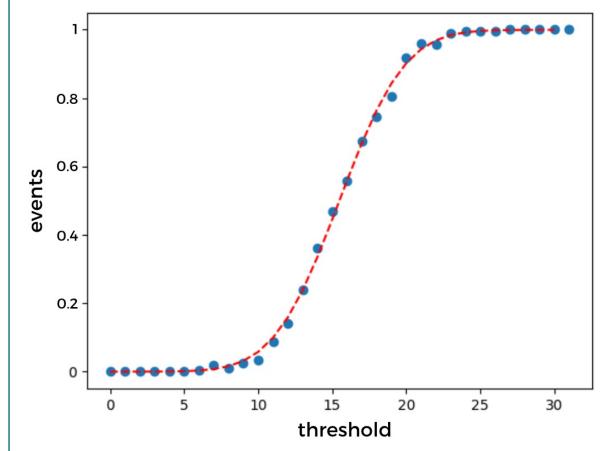
Time measurement:

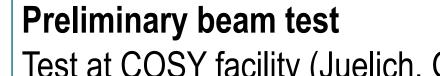


Two threshold:

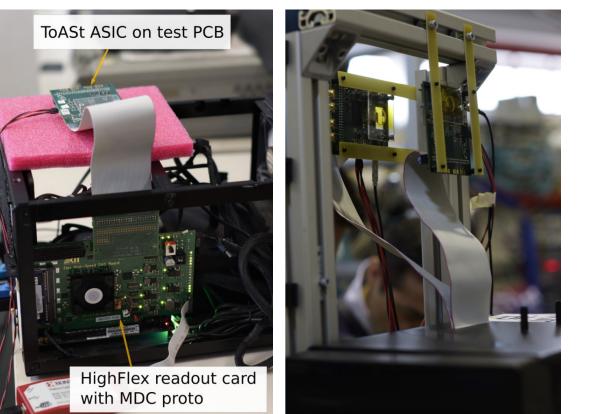
Ο

• store the time stamp on the low threshold (Vth_T) validate it with the high threshold (Vth_E)

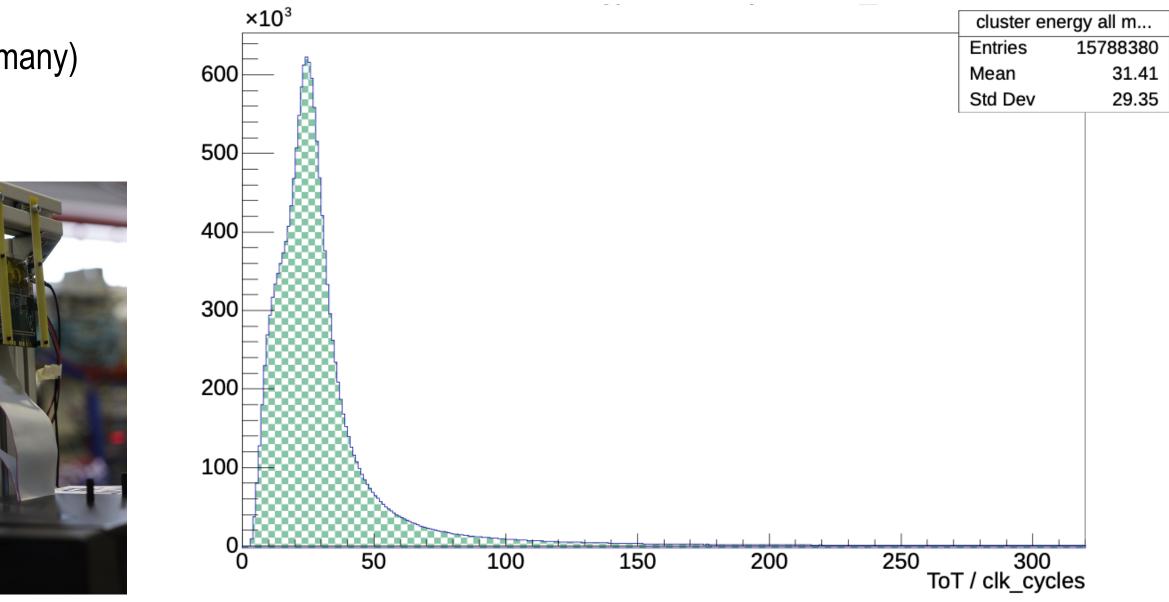


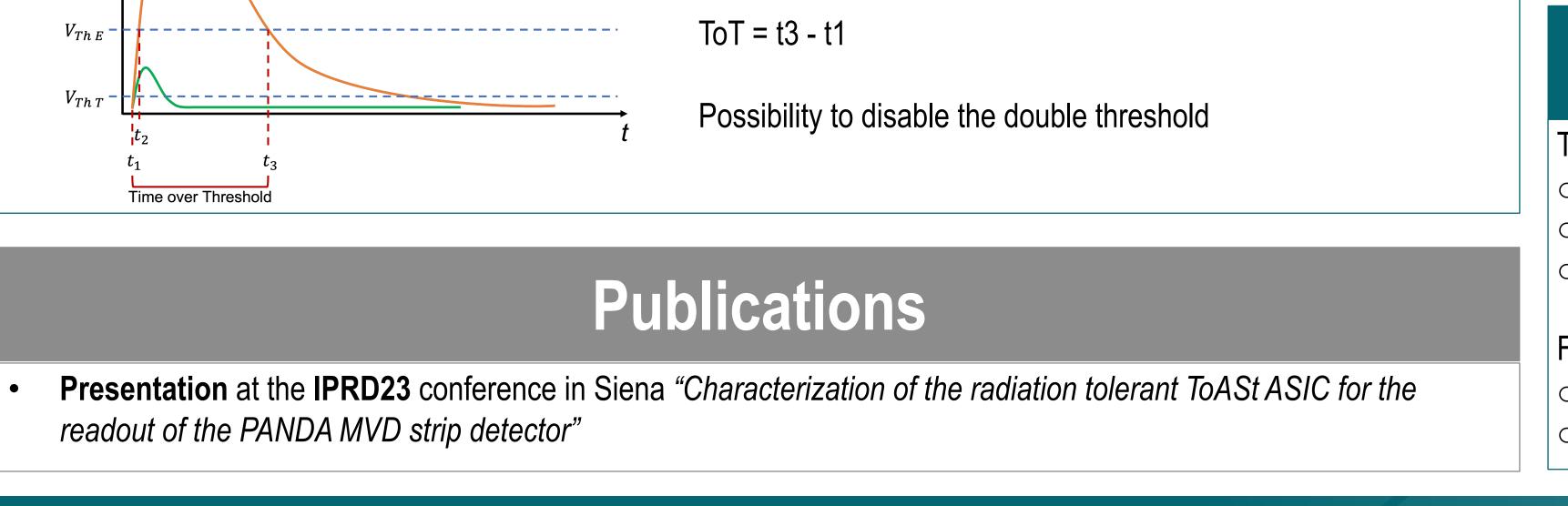


Test at COSY facility (Juelich, Germany) Data collected are under analysis



channe





Future work

Test:

- Performances are as expected
- Tested with detector under preliminary beam test \rightarrow results under analysis Ο
- Test for radiation tolerance (TID and SEU) are not fully satisfying \rightarrow improvement required Ο

Future works:

• Beam test data analysis

• Next version of ToASt (ToASt v2)

PhD program in **Electrical, Electronics and Communications Engineering**