P.hD first year presentation

Real-time DSST and VLSI Architectures for RISC-V Implementation

Supervisors: Prof. Maurizio Martina
Prof. Guido Masera

Student: WALID WALID (278294)

Department of Electronic Engineering

Contents

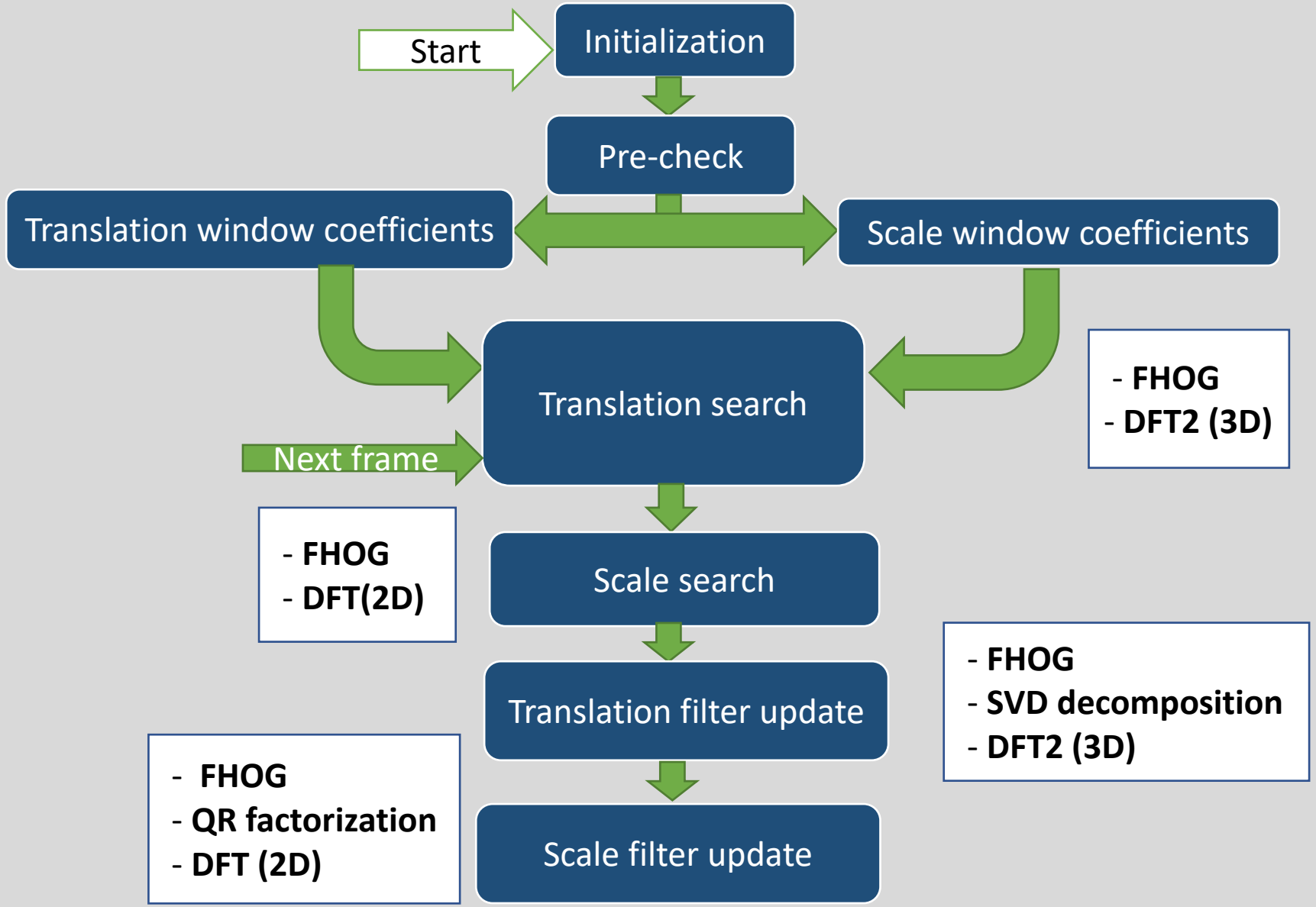
Introduction

- Research Area:
  - Image processing, Visual object tracking, VLSI based architectures, RISC-V.
- Motivation:
  - Huge amount of data processing
  - Computer based solutions are slow
  - Need fast solution for operating in real time
  - Hence hardware acceleration
  - Parallel processing in CPUs
- Applications:
  - Surveillance, Robotics, VAR, Road Scene understanding etc.

- Objectives:

  Hardware implementation strategies in terms of:
  - Dimension complexity
  - Area
  - Performance.

DSST Algorithm

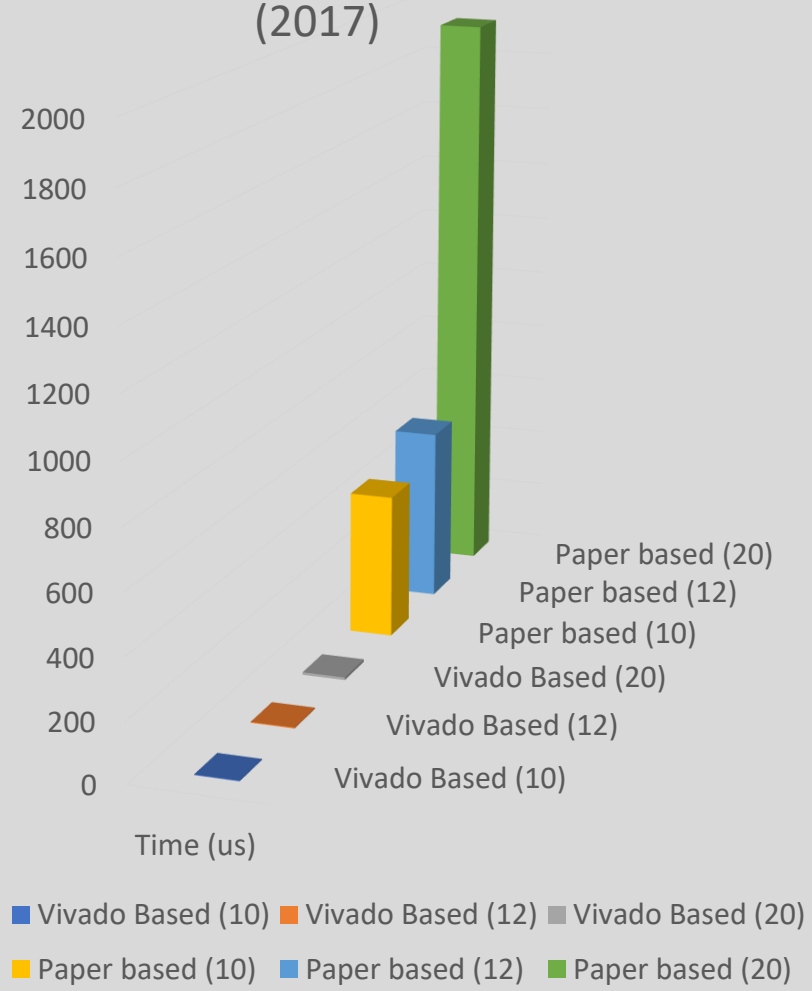


Discriminative Scale Space Tracker (DSST) [1] Danelljan et al, in IEEE, 2016

Results and Discussion

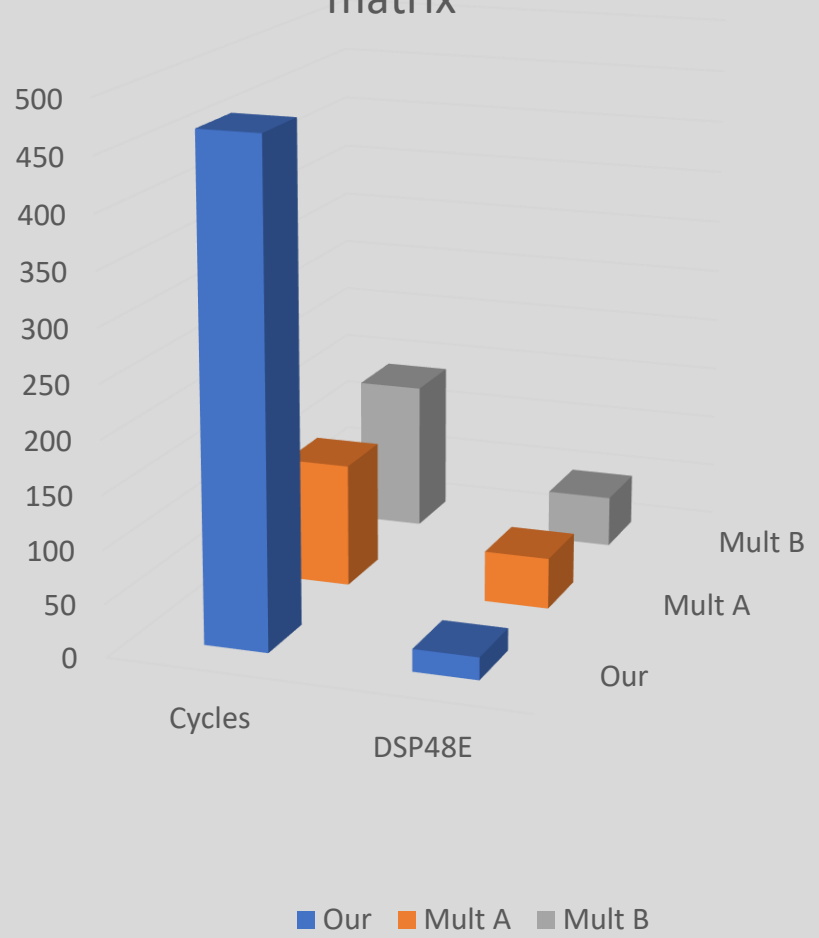
DFT

Timing results: Our and [2] Debaprasad et al, in AMSE journals, (2017)



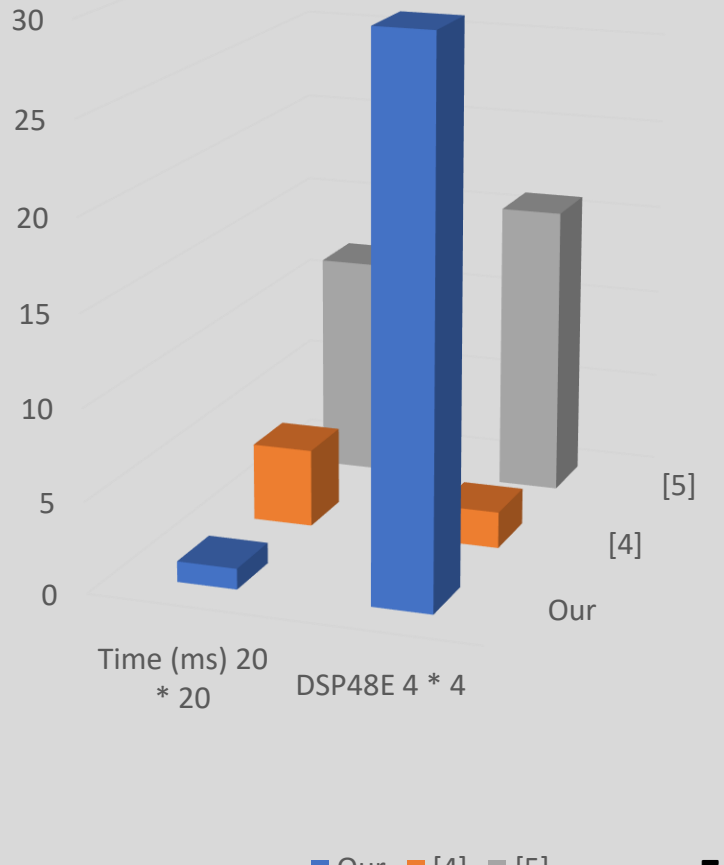
QR

Results: Our and of [3] Sergio D. Muñoz et al, in IEEE, (2015) of 4 * 4 matrix



SVD

Results: Our and of [4,5] Merchant et al, in IERI, (2015), Shiri et al, in ICEE, (2019)



VLSI architectures for RISC-V

- **Literature Review:**
  Cache implementation, Tomasulo Architecture,
  Branch Prediction

- **Current Work:**
  Design of Control Unit for RISC-V out-of-order processor

- **Future Work:**
  OS-complaint RISC-V implementation

References

- [1] Danelljan, M., Häger, G., Khan, F.S., et al.: Discriminative scale space tracking, IEEE Trans. Pattern Anal. Machine Intell., 39(8), 1561-1575 (2016)

- [2] De, D., G.K.K., Ghosh, R., et al.: FPGA implementation of discrete Fourier transform using CORDIC algorithm, Advances in Modelling and Analysis B, 60(2), 332-337 (2017)

- [3] Muñoz, S.D. and Hormigo, J.: High-throughput FPGA implementation of QR decomposition, IEEE Trans. Circ. Syst. II, 62(9), 861-865 (2015)

- [4] Merchant, F., Vatwani, T., Chattopadhyay, A., et al.: Design and performance analysis of fixedpoint Jacobi SVD algorithm on recongurable system, IERI Procedia, 7, 21-27 (2015)

- [5] Shiri, A. and Khosroshahi, G.K.: An FPGA Implementation of Singular Value Decomposition'. 27th Iranian Conference on Electrical Engineering, Yazd, Iran, 416-422 (2019)