

PROBLEM

Different standards for testing Printed Circuit Boards (PCBs) during their production and operational life are defined, in particular for safety-critical applications (e.g., the automotive field). Some test mechanisms are used for testing the digital electronics at the end of production and in-field. Assessing the effectiveness of test mechanisms is only possible after a fault model is defined; for example, the stuck-at fault model is widely used in digital electronics. Currently, the scientific and industrial community is looking for suitable fault models for the analog and power circuits as well. The definition of an analog fault model would allow us to evaluate the effectiveness of analog test strategies. Presently, the effectiveness of the test procedures is performed in a qualitative way [3], e.g., by the electrical parameters of the Device Under Test (DUT).

The purpose of the Ph.D. activity is to devise possible metrics able to assess the real effectiveness of test strategies

in a quantitative way

i.e., computing a Fault Coverage figure considering a fault model (catastrophic faults) [1][2].

STATE OF THE ART

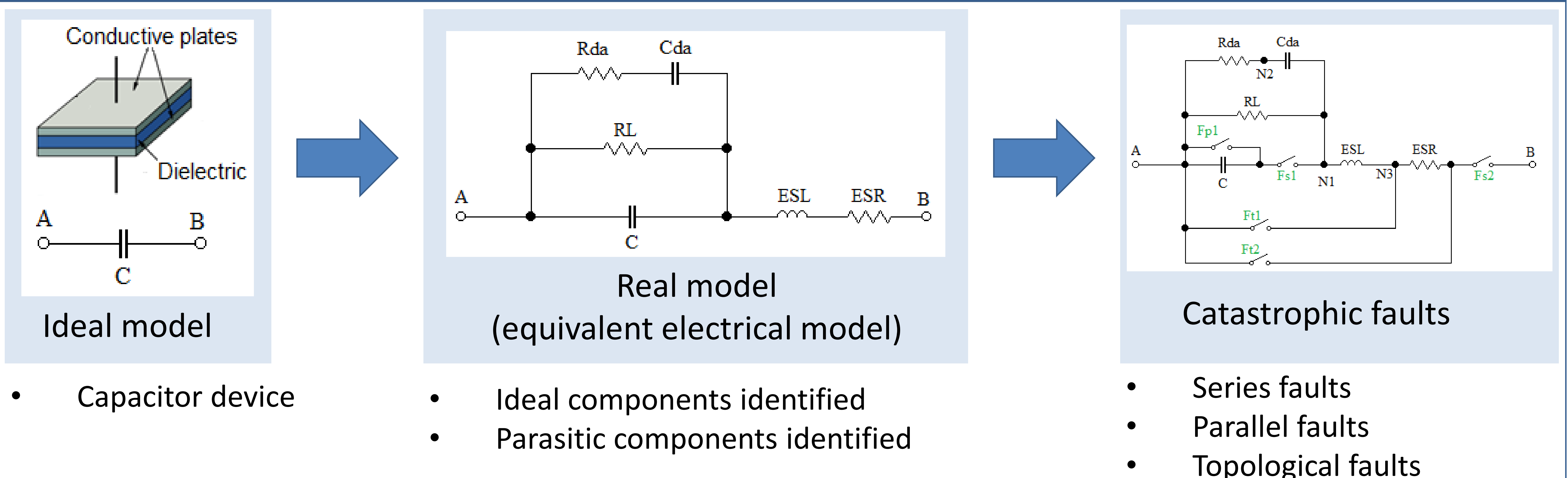
Metrics currently used

- PCOLA
- Sensitivity approach
- Monte Carlo analysis
- New commercial fault simulation tools (e.g., Mentor's DefectSim and Synopsys's TestMAX)

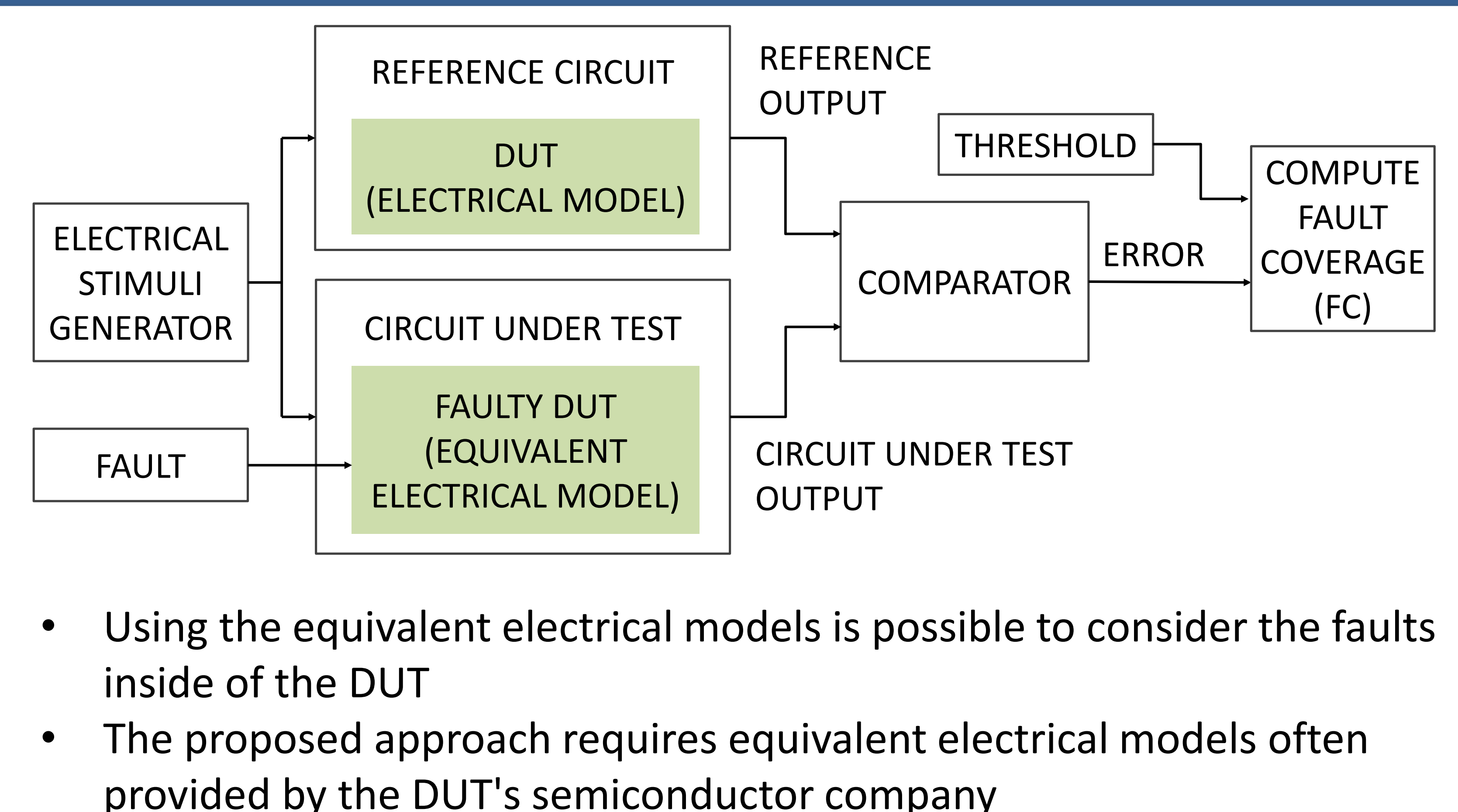
Test strategies

- Incoming inspection test
- In-circuit test
- Functional test
- Thermal monitoring test

PROPOSED APPROACH – (a) Generate the fault list



PROPOSED APPROACH – (b) Perform Fault simulation



CONCLUSIONS

The proposed approach uses a circuit simulator to **evaluate the FC**. Moreover, a strategy able to identify the possible catastrophic faults in the equivalent electrical model of the DUT is proposed. To evaluate the effectiveness of the proposed approach, **the FC achieved by different test procedures on different DUT is evaluated**. Different test strategies are considered and compared. From the results obtained, it is possible to **rank the test methods**. Furthermore, it is possible to **identify the redundant tests**.

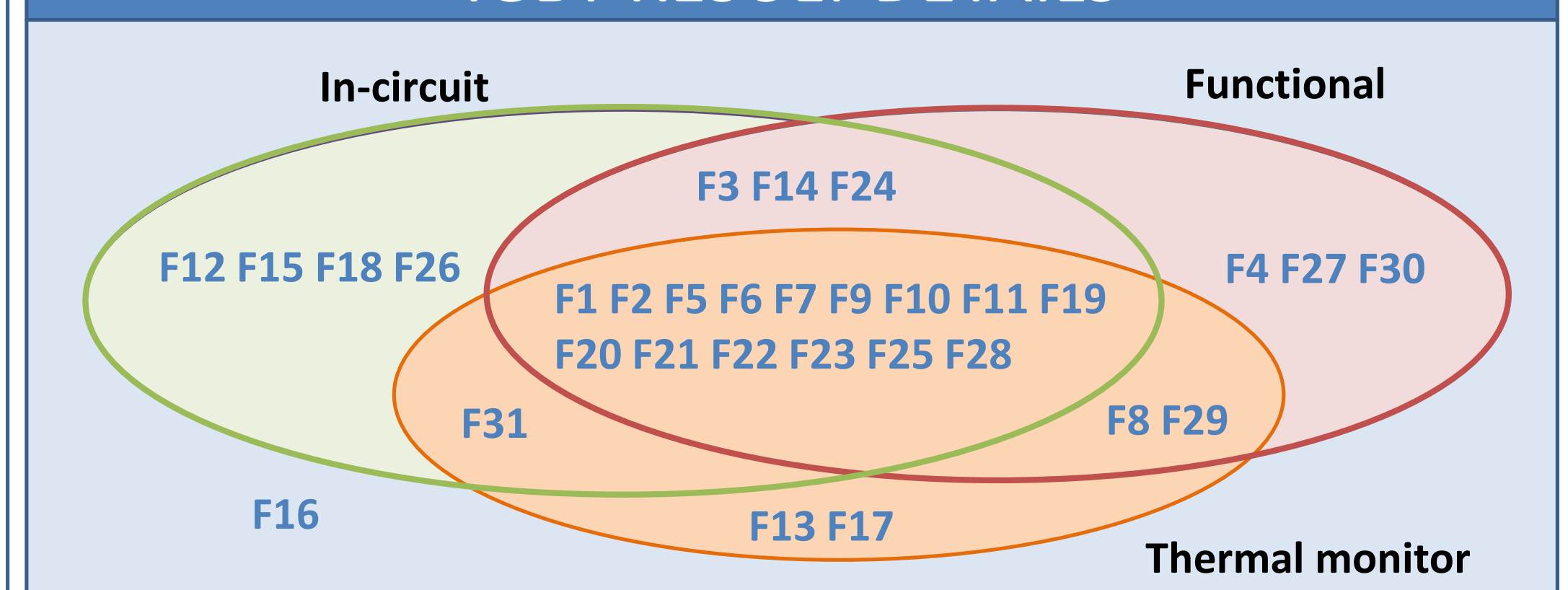
RESULTS

Case study

- Power Supply Unit (PSU) used in industrial compressors (400V – 12A)
- Boost cell
- IGBT, Diode, BJT

Device	#catastrophic faults	#fault detected			
		In-circuit	Functional	Thermal monitoring	Total
IGBT	31	23	23	20	30
Diode	4	1	4	1	4
MOSFET	27	22	22	14	25

IGBT RESULT DETAILS



Contact

Davide Piumatti
Politecnico di Torino
CAD Group
Email: davide.piumatti@polito.it
Website: www.cad.polito.it

References

1. D. Piumatti and M. Sonza Reorda, "Assessing Test Procedure Effectiveness for Power Devices," 2018 Conference on Design of Circuits and Integrated Systems (DCIS), Lyon, France, 2018, pp. 1-6.
2. D. Piumatti, S. Borlo, F. Mandrile, M. Sonza Reorda, R. Bojoi, "Assessing the Effectiveness of the of Power Devices at the Board Level," 2019 Conference on Design of Circuits and Integrated Systems (DCIS), Bilbao, Spain, 2019, IN PRESS.
3. Wai Chen, "The Electrical Engineering Handbook," Academic Press Book, 2005, ISBN 9780080477480.